REMARKS

In response to the Office Action mailed July 26, 2006, Applicant respectfully requests reconsideration. To further the prosecution of this Application, Applicant submits the following remarks and has added new claims. The claims as now presented are believed to be in allowable condition.

Claims 1-20 were pending in this Application. Claims 21-25 have been added. Accordingly, claims 1-25 are now pending in this Application. Claims 1, 6, 13, and 14 are independent claims.

Rejections under §103

Claims 1, 6, 13, and 14 were rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,333,650 (Amin, et al.) in view of U.S. Patent No. 6,879,139 (Brown, et al.). Claims 2-5, 7-12, and 15-20 were rejected under 35 U.S.C. §103(a) as being unpatentable over Amin and Brown, in further view of U.S. Patent No. 6,850,048 (Orr, et al.). Applicant respectfully traverses each of these rejections and requests reconsideration. The claims are in allowable condition.

Amin discloses a voltage sequencing circuit 103 to sequentially power-up an electrical system requiring multiple voltage levels (Abstract and column 2, lines 34-35). The voltage sequencing circuit 103 contains power regulators 120-122 and a control sequencing component 123 (column 2, lines 52-55). The power regulators 120-122 receive power from a main power supply source 130 and convert that power into different output voltage signals (column 2, lines 58-64). The main power supply source 130 feeds the power to the power regulators 120-122 through a main power signal V_{in} (Figure 1). The control sequencing component 123 monitors the outputs of the power regulators 120-122 and activates enable signal lines 126, connected to the power regulators 120-122 to instruct each power regulator when to operate (column 2, line 65 through column 3, line 16). The power output of each power regulator powers circuits 110-112 of

an electrical system 101 each at a different voltage (column 2, lines 55-64). In order to activate a power-up sequence, the enable signals are first deactivated (column 3, lines 33-34). Main power is applied from the main power supply source 130 over signal V_{in} (column 3, lines 36-37). The control sequencing component 123 waits a preset period of time for V_{in} to settle and then activates the enable signal 126 for the first power regulator 120 (column 3, lines 37-42). This causes the first power regulator 120 to output a power signal to circuit 110 (column 3, lines 42-44). Once the first power signal settles, the control sequencing component 123 enables subsequent power regulators in a similar manner (column 3, lines 45-57). The control sequencing component 123 also monitors all the power signals for errors (column 3, lines 58-65).

Orr discloses a power supply controller 10 having a first and a second control unit 21, 22 and an isolating signal coupler 23 (Abstract). Orr also discloses NVRAM 26 coupled to the second control unit 22 (column 7, lines 1-5). This NVRAM 26 stores information about the input voltage Vin, the sequence of enabling power supplies 11-16 attached to the power supply controller 10, and parameters of the power supplies 11-16 (column 10, lines 43-45). Upon initialization, data is transferred from the NVRAM 26 to shadow registers on converter state machines (CSM) 42 and input state machines 43 located on the power supply controller 10 (column 10, lines 45-51). The NVRAM stores a start-up identifier for each CSM 42 and its associated power supply 11-16 (column 11, lines 8-20). This start-up identifier identifies the CSM 42 or other state machine that precedes the CSM 42 at issue, as well as a time delay period (column 11, lines 21-24 and column 12, line 4-15). In addition, the NVRAM may store information about faults in the input voltage Vin or in any of the power supplies 11-16 (column 12, line 62 through column 13, line 6).

Brown discloses a method for enabling and disabling power supplies in sequence (Abstract). A secondary control unit 12 monitors the outputs Vout1-Vout6 of several power supplies 1-6, and a primary control unit 11 controls the

operation of each of the power supplies 1-6 through enable inputs E (column 4, lines 38-46).

Claims 1, 6, 13, and 14 were rejected under 35 U.S.C. §103(a) as being unpatentable over Amin in view of Brown. Taking claim 6 as an example, claim 6 is directed to a *packaged microcontroller* for controlling a data storage system having power circuitry for providing power signals and storage processing circuitry for performing data storage operations. The packaged microcontroller has a set of input lines; a set of output lines; and control circuitry coupled to the set of input lines and the set of output lines. The *control circuitry is configured to receive, on the set of input lines, a first set of power signals which is provided by the power circuitry to the storage processing circuitry*, wait a predetermined time period in response to receipt of the first set of power signals on the set of input lines, and output, through the set of output lines, a set of enable signals to the power circuitry after waiting the predetermined time period, the set of enable signals directing the power circuitry to provide a second set of power signals to the storage processing circuitry.

The cited references do not teach or suggest, either alone or in combination, a *packaged microcontroller* for controlling a data storage system. Amin nowhere even mentions packaged microcontrollers. The Office Action, on page 4, identifies the voltage sequencing circuit 103 of Amin as a packaged microcontroller. However, even if the voltage sequencing circuit 103 serves some of the same functions as the *packaged microcontroller* of claim 6, nowhere does Amin teach that the voltage sequencing circuit 103 is a *packaged microcontroller.* Indeed, there are significant advantages to utilizing a *packaged microcontroller* in order to control the power delivery to a set of storage processing circuits. As pointed out in the specification, "use of the packaged microcontrollers 36 provide flexibility in that changes to their operation (e.g., modification for a bug fix, upgrades, etc.) can be made by simply replacing the codes in their memories with new codes" (Page 6, lines 25-27). In addition, "in contrast to discrete

component configurations for power sequencing, use of the packaged microcontrollers 36 is inexpensive and requires minimal circuit board space since the packaged microcontrollers 36 are essentially standard parts disposed in a relatively small package[]" (Page 7, lines 1-4). These advantages are not noted in Amin because Amin does not anticipate using a *packaged microcontroller*. Moreover, it is unclear why one would want to modify Amin to use a *packaged microcontroller* since implementing Amin by using a *packaged microcontroller* would likely be ineffective. In particular, if the voltage sequencing circuit 103 of Amin were implemented as a packaged microcontroller, it would have to accept a large amount of power from the main power supply source 130 and supply power to multiple electrical circuits 110-112. Packaged microcontrollers are not suited to transmitting such large amounts of power, as the large amounts of power traveling through such a small footprint may make the packaged microcontroller overly susceptible to overheating.

In addition, the cited references do not teach or suggest, either alone or in combination, *control circuitry configured to receive, on the set of input lines, a first set of power signals which is provided by the power circuitry to the storage processing circuitry*. The Office Action, on page 4, identifies the control sequencing component 123 of Amin as the *control circuitry* of claim 6 and the signal V_{in} and the input from control component 135 of Amin as the *set of input lines* of claim 6. The Office Action also identifies, on page 4, the main power supply source 130 of Amin as the *power circuitry* of claim 6 and circuits 110-112 of Amin as the *storage processing circuitry* of claim 6. However, the control sequencing component 123 does not receive a *first set of power signals* from the main power supply source 130 over V_{in} and the input from control component 135. Control sequencing component 123 does receive one power signal from the main power supply source 130 over V_{in}, but that signal inputs into the power regulators 120-122 of the voltage sequencing circuit 103. There is no indication that it also inputs into the control sequencing component 123. Furthermore, even if control sequencing component 123 does receive V_{in}, control sequencing

component 123 still would not receive a *set of power signals* over V_{in} and the input from control component 135, but rather merely one power signal. In addition, the *first set of power signals* is not *provided by the power circuitry to the storage processing circuitry*, since the main power supply source 130 does not send power signals to circuits 110-112, but rather the voltage regulators 120-122 provide the power signals to circuits 110-112.

For the reasons stated above, claim 6 patentably distinguishes over the cited prior art, and the rejection of claim 1 under 35 U.S.C. §103(a) should be withdrawn. Accordingly, claim 6 is in allowable condition.

Since claims 1, 13, and 14 were rejected for similar reasons as claim 6, claims 1, 13, and 14 are also in allowable condition for similar reasons as is claim 6.

Because claims 2-5 depend from and further limit claim 1, claims 2-5 are in allowable condition for at least the same reasons as claim 1. Because claims 7-12 depend from and further limit claim 6, claims 7-12 are in allowable condition for at least the same reasons as claim 6. Because claims 15-20 depend from and further limit claim 14, claims 15-20 are in allowable condition for at least the same reasons as claim 14.

Additionally, it should be understood that the dependent claims recite additional features which further patentably distinguish over the cited prior art. For example, claim 3 recites wherein the packaged microcontroller further includes memory which stores *pre-loaded code having a version identifier*, the control circuitry being configured to *compare the version identifier of the pre-loaded code with a version identifier of available new code*, and *replace the pre-loaded code stored in the memory with the available new code when the version identifier of the available new code indicates that the available new code is newer than the pre-loaded code, and maintain the pre loaded code within the memory when the version identifier of the available new code indicates that the available new code is not newer than the pre-loaded code*. These features are not taught or suggested by the cited prior art. Orr discusses start-up identifiers (see, e.g.,

column 12, lines 4-15), however, there is no mention of a *version identifier*. Furthermore, there is no mention in Orr of any comparison between *the version identifier of the pre-loaded code with a version identifier of available new code*, nor is there any mention of replacing or maintaining the pre-loaded code depending on such a comparison. If the rejection of claim 3 is to be maintained, Applicant respectfully requests that it be pointed out with particularity where the cite prior art teaches *pre-loaded code having a version identifier*, the control circuitry being configured to *compare the version identifier of the pre-loaded code with a version identifier of available new code*, and *replace the pre-loaded code stored in the memory with the available new code when the version identifier of the available new code indicates that the available new code is newer than the pre-loaded code, and maintain the pre loaded code within the memory when the version identifier of the available new code indicates that the available new code is not newer than the pre-loaded code*.

As another example, claim 4 recites wherein the packaged microcontroller further includes a *dedicated memory location*, wherein the control circuitry, when replacing the pre-loaded code stored in the memory with the available new code, is configured to *set the dedicated memory location with a flag to indicate that a code replacement routine is in progress*, *overwrite the pre-loaded code* stored in the memory with the available new code, and *clear the dedicated memory location to remove the flag to indicate that no code replacement routine is in progress*. These features are not taught or suggested by the cited prior art. If the rejection of claim 4 is to be maintained, Applicant respectfully requests that it be pointed out with particularity where the cited prior art teaches these features.

As another example, claim 10 recites a *dedicated memory location*, and

memory having *a main portion which stores pre-loaded main code and a secondary portion which stores pre-loaded secondary code*, wherein the control circuitry is further configured to access the dedicated memory location to determine whether a flag is set to indicated that a code replacement routine is in progress, and run (i) the pre-loaded main code stored in the main portion of the

memory when the dedicated memory location is not set with the flag, and (ii) the secondary code stored in the secondary portion of the memory when the dedicated memory location is set with the flag. These features are not taught or suggested by the cited prior art. If the rejection of claim 10 is to be maintained, Applicant respectfully requests that it be pointed out with particularity where the cited prior art teaches these features.

Newly Added Claims

Claims 21-25 have been added and are believed to be in allowable condition. Claims 21-23 depend from claim 1. Claims 24-25 depend from claim 6. Support for claim 21 is provided within the Specification, for example, on page 5, lines 20 through 24. Support for claims 22 and 24 is provided within the Specification, for example, on page 5, lines 24 through 26 and on page 9, lines 19 through 27. Support for claims 23 and 25 is provided within the Specification, for example, on page 7, lines 19 through 28.

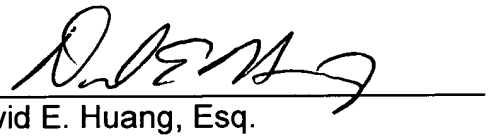
Conclusion

In view of the foregoing remarks, this Application should be in condition for allowance. A Notice to this affect is respectfully requested. If the Examiner believes, after this Amendment, that the Application is not in condition for allowance, the Examiner is respectfully requested to call the Applicant's Representative at the number below.

Applicant hereby petitions for any extension of time which is required to maintain the pendency of this case. If there is a fee occasioned by this Amendment, including an extension fee that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 50-3661.

If the enclosed papers or fees are considered incomplete, the Patent Office is respectfully requested to contact the undersigned collect at (508) 616-2900, in Westborough, Massachusetts.

Respectfully submitted,



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